REMARKS

New Claims 29-42 are added. Claims 1, 3, 18, and 20-42 are pending. Claims 1, 3, 18, and 21-25 are amended. No new matter is added by the claim amendments.

Claims 18, 20, and 26-28 are allowed, and Claims 22 and 24-25 are allowable. Applicants thank the Examiner for allowing those claims.

35 U.S.C. § 103(a)

The Office Action mailed August 13, 2009, states that Claims 1, 3, 21, and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Application No. 02-054058 by Koichi in view of United States Patent No. 5,437,017 by Moore et al. ("Moore"). Applicants have reviewed the cited references and respectfully submit that the embodiments of the present invention recited in Claims 1, 3, 21, and 23 are patentable over Koichi and Moore, alone or in combination.

Applicants respectfully submit that Koichi does not show or suggest an indication that a target instruction has been translated into a host instruction, as recited in the claims. Specifically, Applicants respectfully submit that Koichi does not show or suggest "means for providing an indication whether a first memory address to be written stores a target instruction for a first instruction set architecture which has been translated to at least one host instruction for a second instruction set architecture, the at least one host instruction stored at a second memory address, the means for providing comprising: a look-aside buffer including a plurality of storage locations … including a first storage location

for the first memory address, and a storage position corresponding to the first storage location for storing the indication" as recited in independent Claim 1.

According to the Office Action mailed August 13, 2009, "converted" is being read as "translated." Applicants disclaim the remarks included in the response to that Office Action regarding the distinction between "translated" and "converted." Nevertheless, Applicants do not admit that "converted" and "translated" are synonymous. According to Claim 1, instructions are translated from a first instruction set architecture to a second instruction set architecture. Koichi does not show or suggest translating an instruction as recited in Claim 1.

Furthermore, regardless of whether an instruction is converted or translated, Koichi makes no mention of the claimed indication in association with the instruction.

According to page 6 of the Office Action mailed August 13, 2009, the claimed indication is embedded in the system of Koichi. However, there is no teaching or even a suggestion in Koichi that the claimed indication is embedded in Koichi's system.

Applicants respectfully submit that there is no showing or suggestion in the reference that Koichi's system stores a translated (e.g., host) instruction. Also, Applicants respectfully submit that there is no showing or suggestion in the reference that Koichi's system stores a memory address that stores a non-translated (e.g., target) instruction. Furthermore, Applicants respectfully submit that there is no showing or suggestion in the reference that Koichi's system

stores, with a memory address for a non-translated instruction, an indication that the non-translated instruction at that memory address has been translated.

In summary, Applicants respectfully submit that Koichi is lacking in many respects. It would appear that the Examiner's interpretation of Koichi is a strained attempt to make Koichi read on the claimed invention. Applicants respectfully submit that such an interpretation could be made only by hindsight gleaned from the Applicants' own disclosure, and of course such hindsight is impermissible.

Applicants respectfully submit that Moore does not overcome the shortcomings of Koichi. As understood by the Applicants, Moore only maintains coherency between a virtual address and a physical address translated from the virtual address. However, the claimed indication is not concerned with the translation between a virtual address and a physical address. As noted above, the claimed indication pertains to the translation between a target instruction and a host instruction.

In summary, Applicants respectfully submit that Koichi and Moore, alone or in combination, do not show or suggest the features of Claim 1 cited above. Therefore, Applicants respectfully submit that the basis for rejecting Claim 1 under 35 U.S.C. § 103(a) is traversed and that Claim 1 is in condition for allowance.

Each of the Claims 3, 21, and 23 includes all of the features of Claim 1 plus additional features. Applicants respectfully submit that Koichi and Moore do not show or suggest the features of Claims 3, 21, and 23 in combination with the features of Claim 1, and also that Claims 3, 21, and 23 are in condition for

allowance at least because they depend from an allowable claim. Consequently, the Applicants respectfully assert that the basis for rejecting Claims 3, 21, and 23 under 35 U.S.C. § 103(a) is also traversed.

Conclusions

In light of the above remarks, Applicants respectfully request reconsideration of the rejected claims. Based on the arguments presented above, Applicants respectfully assert that Claims 1, 3, 21, and 23, as well as new Claims 29-42, overcome the rejections of record and, therefore, Applicants respectfully solicit allowance of these claims.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present application.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
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